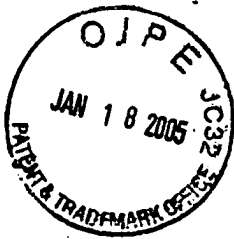


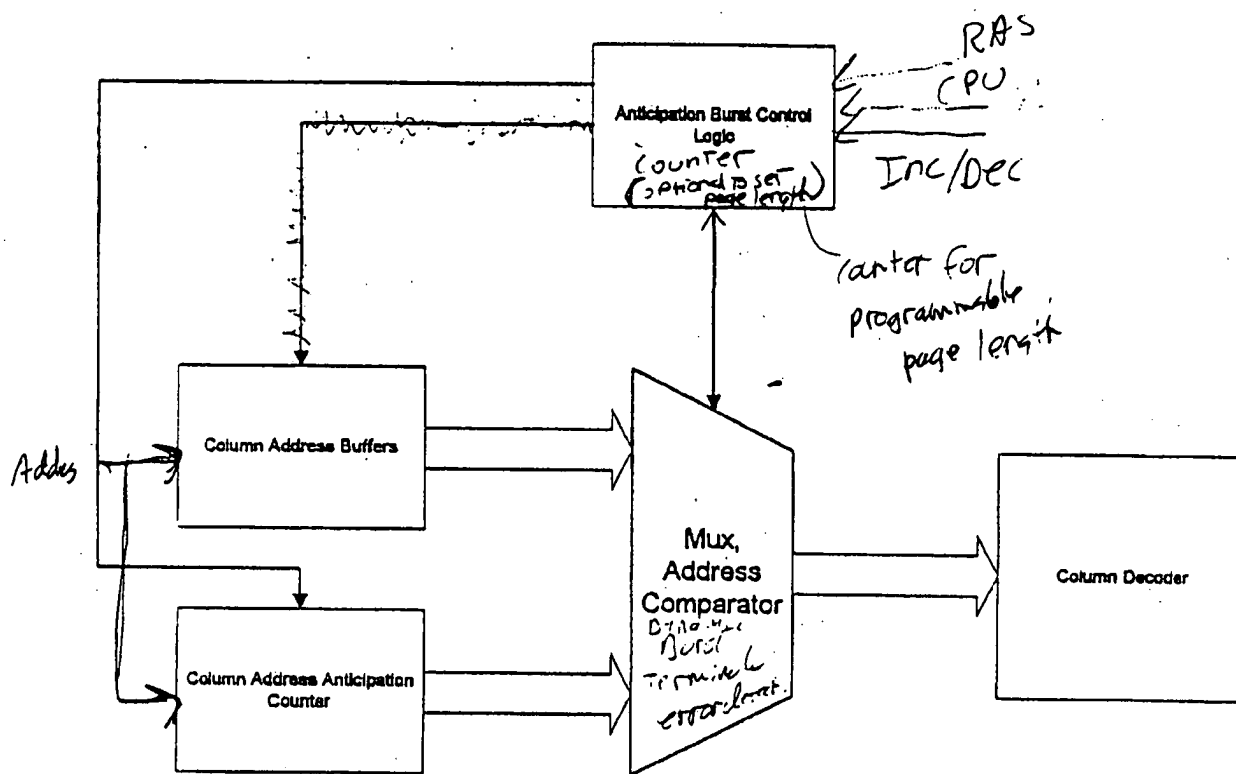
Exhibit B



BEST AVAILABLE COPY

P.3

3 of 4



Memory System Speed Enhancement
Block Diagram

Erik Erlandson, David Tremblay



Value

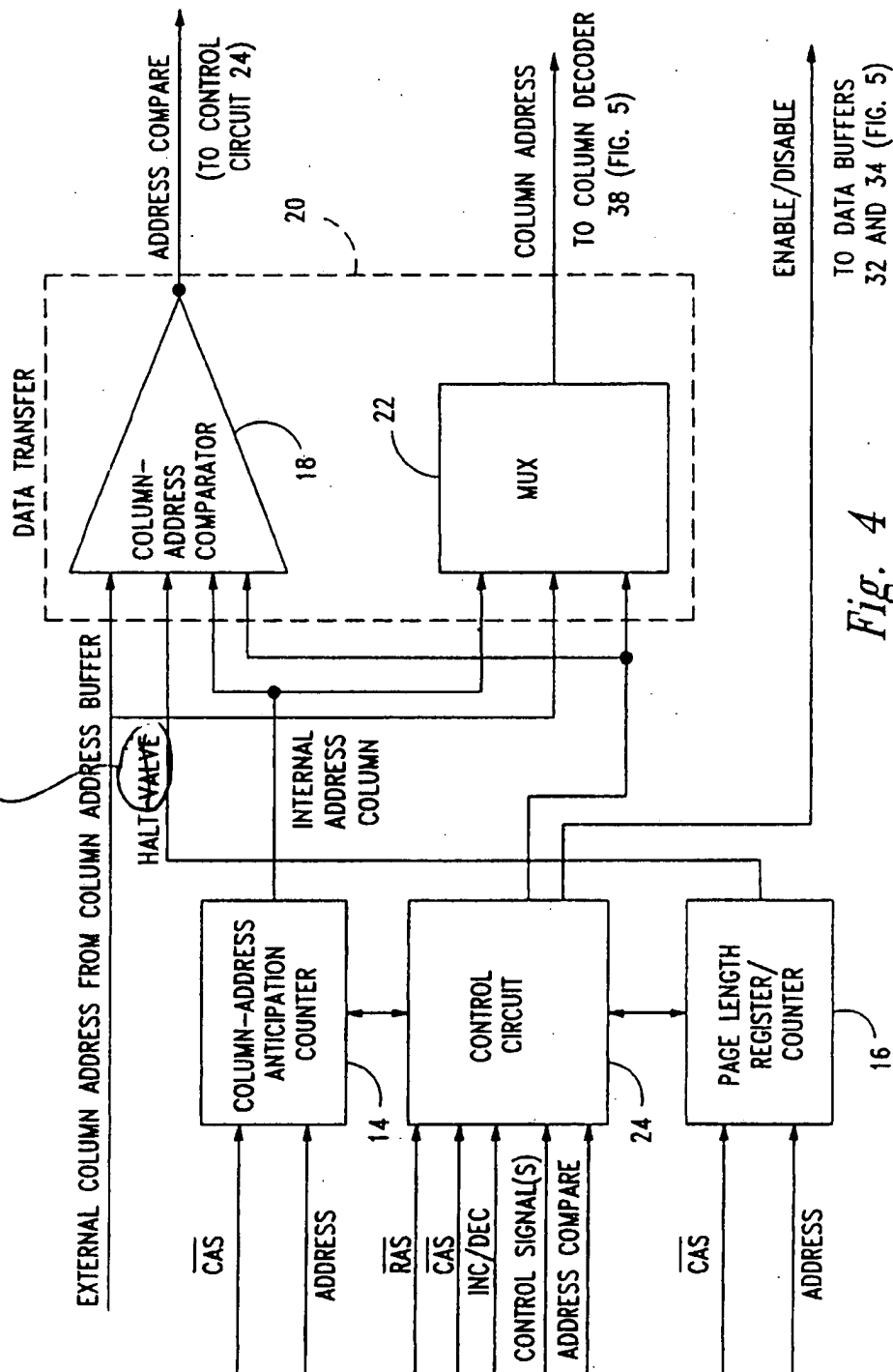


Fig. 4